

Interference

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|----|------|-----|------|--|----------|------------------|
| 1 | BRS | L2 | 5 | (cad same verif\$3) and (simulat\$3 adj model) and (HDL) | US-PGPUB | 2006/05/16 12:44 |
| 2 | BRS | L3 | 0 | (cad same verif\$3).clm. and (simulat\$3 adj model) and (HDL).clm. | US-PGPUB | 2006/05/16 12:44 |
| 3 | BRS | L4 | 0 | (cad same verif\$3).clm. and (HDL).clm. | US-PGPUB | 2006/05/16 12:44 |
| 4 | BRS | L1 | 138 | (cad same verif\$3) and (simulat\$3 adj model) | US-PGPUB | 2006/05/16 12:50 |
| 5 | BRS | L5 | 0 | (instatiat\$3 same instruction).clm. | US-PGPUB | 2006/05/16 12:50 |
| 6 | BRS | L6 | 68 | (instantia\$4 same instrumentation) | US-PGPUB | 2006/05/16 12:51 |
| 7 | BRS | L7 | 9 | (instantia\$4 same instrumentation).clm. | US-PGPUB | 2006/05/16 12:53 |
| 8 | BRS | L8 | 39 | (input adj mapping).clm. | US-PGPUB | 2006/05/16 12:54 |
| 9 | BRS | L9 | 0 | (input adj mapping).clm. and (HDL).clm. | US-PGPUB | 2006/05/16 12:54 |
| 10 | BRS | L10 | 0 | (input adj mapping).clm. and (circuit adj design).clm. | US-PGPUB | 2006/05/16 12:54 |
| 11 | BRS | L11 | 1 | (input adj mapping).clm. and (circuit adj design)". | US-PGPUB | 2006/05/16 12:56 |
| 12 | BRS | L12 | 10 | (signal adj overrid\$3).clm. and (signal same enable).clm. | US-PGPUB | 2006/05/16 12:57 |

TS

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|--|---|------------------|
| 1 | BRS | L18 | 0 | ibm.as. and (cad same hdl) | US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB | 2006/05/16 13:12 |
| 2 | BRS | L19 | 1 | ibm.as. and (cad and hdl) | US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB | 2006/05/16 13:12 |
| 3 | BRS | L20 | 0 | ibm.as. and (non adj conventional adj HDL) | US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB | 2006/05/16 13:13 |
| 4 | BRS | L21 | 1 | (non adj conventional adj HDL) | US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB | 2006/05/16 13:13 |